REMARKS/ARGUMENTS

These remarks are offered in response to the Office Action of November 3, 2004 (Office Action). Applicant respectfully requests a one month retroactive extension of time, a petition for which and the appropriate fee are filed with this response to the Office Action.

In the Office Action, Claims 1-6 were rejected under 35 U.S.C. § 112, first paragraph, for failing to satisfy the enablement requirement. Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,313,174 to White (White).

Applicant, as an initial matter, wishes to thank the Examiner for a thorough examination of the application. Claims 1-6 have been cancelled and Claims 7-12 are hereby added. The newly added claims are fully supported in the Specification, as detailed herein.

FIG. 1 has been amended to clarify the procedure illustrated therein in response to the Examiner's remarks. A marked-up copy of the amended drawing indicating the change is attached hereto under the heading "Replacement Sheet." and a detailed explanation of the how the change alters the drawing is provided below.

Page 10 of the Specification has been amended to correct an inconsistency with a portion of FIG. 1. The amended portion of the Specification does not relate in any manner to the correction made in the drawing.

The amendments are fully supported in the specification. No new matter has been added by virtue of any of these amendments.

I. Applicant's Invention

It may be helpful to summarize certain aspects of the Applicant's invention prior to addressing the Examiner's rejection based on the cited reference. One embodiment of the invention is a high-speed scalable multiplier. As recited in Claim 7 and described

particularly at pages 11 and 12 of the Specification, the high-speed scalable multiplier can include at least one folding multiplier. As further described in the specification, the folding multiplier is used to perform a "folding process." (Specification; see, particularly, pp. 8 and 12.) It is explicitly stated at page 7 of the Specification that the term "folding" is intended to mean "programmatically reducing the size of [a] multiplicand, multiplier, or both until the reduced multiplicand and multiplier are below a threshold." As described at pages 7 and 10 of the specification, the folding process that is effected by the folding multiplier generates a "folded product" that utilizes less computing resources, reduces power dissipation, and yet renders an uncorrupted multiplication result.

Functionally, the folded product is generated by a "folding process" explicitly described at pages 8 through 10 of the Specification, wherein it is also explicitly stated that the process can be performed by the folding multiplier. The process, as described, begins with the generation of a first folding value based on an average of the multiplicand and the multiplier, along with the generation of a second folding value based on one-half a difference of the multiplicand and the multiplier. (Specification, pp. 8-9.) As set forth in the Specification, the multiplicand and the multiplier can be designated x and y, respectively. The first folding value, designated P in the specification, is therefore $P=\left(\frac{x+y}{2}\right)$, and the second folding value, designated Q, is accordingly $Q=\left(\frac{x-y}{2}\right)$.

The process, as further described, includes generating a first square based upon a squaring of a difference between the first folding value and a portion of a first scaling factor, and generating a second square based upon a squaring of a difference between the second folding value and a portion of a second scaling factor. (Specification, p. 10.)

Carrying out the operations yields the following results, where, as in the Specification, A designates the first folding value and B designates the second folding value:

$$A=\left(P-K/2\right)^2=\left[\frac{(x+y)}{2}-\frac{K}{2}\right]^2=\left(\frac{x+y}{2}\right)-(x+y)\left(\frac{K}{2}\right)+\left(\frac{K}{2}\right)^2=\left(\frac{x^2+2xy+y^2}{4}\right)-\frac{xK}{2}-\frac{yK}{2}+\frac{K^2}{4},$$

and

$$B=\left(Q-L/2\right)^2=\left[\frac{(x-y)}{2}-\frac{L}{2}\right]^2=\left(\frac{x-y}{2}\right)^2-(x-y)\left(\frac{L}{2}\right)+\left(\frac{l}{2}\right)^2=\left(\frac{x^2-2xy+y^2}{4}\right)-\frac{xL}{2}+\frac{yL}{2}+\frac{L^2}{4}.$$

Multiplying the first folding value times the first scaling factor generates a first product, C. (Specification, p. 10.) Multiplying the second folding value times the second scaling factor generates a second product, D. (Specification, p. 10.) Algebraically, the results yielded by these operations are: $C=KP=K\left(\frac{x+y}{2}\right)$, and $D=LQ=L\left(\frac{x-y}{2}\right)$.

A third square is generated based upon a squaring of the portion of the first scaling factor, and a fourth square is generated based upon a squaring of the portion of the second scaling factor. (Specification, p. 10.) The folded product is described in the Specification as comprising $A-B+C-D-E+F$, where each of the terms are as described already. (Specification, p. 10.) Note that the difference between the first two terms yields $A-B=xy+x\frac{(L-K)}{2}-y\frac{(K+L)}{2}+\frac{(K^2-L^2)}{4}$, and the difference between the third and fourth terms yields: $C-D=x\frac{(K-L)}{2}+y\frac{(K+L)}{2}=-x\frac{(L-K)}{2}+y\frac{(K+L)}{2}$. Additionally, with respect to the last two terms, their difference is: $-E+F=-\left(\frac{K}{2}\right)^2+\left(\frac{L}{2}\right)^2=-\frac{K^2-L^2}{4}$.

Accordingly, the result of summing the second square, second product, and third square, summing the second square, second product, and third square, and taking the difference between the sums yields XY, which is the product of the original multiplicand and multiplier. Thus, as explicitly stated page 7 of the Specification, the folding process, though initially reducing the size of the multiplicand and multiplier by virtue of dividing by two, nonetheless results in the desired product.

As particularly described at page 9 of the specification, if either the multiplicand or multiplier exceeds a threshold, the folding process results in their sizes being reduced. This is delineated by the algebraic steps set out above wherein the reduction occurs as a result of the inclusion of the scaling factors K and L. Whenever the multiplicand does not exceed the threshold, the scaling factor K is set to zero, as described at page 9 of the Specification and illustrated in block 112 of FIG. 1. Similarly, whenever the multiplier does not exceed the threshold, the scaling factor L is set to zero, as also described at page 9 of the Specification and illustrated in block 118. The result is a more efficient use of processing resources, namely, a reduction in the amount of memory needed to perform the desired multiplication. (Specification, p. 8.)

II. U.S. Patent No. 4,313,174 to White Does Not Anticipate Applicant's Invention

At page 2 of the Office Action, the Examiner rejected Claim 1 under 35 U.S.C. §102(b) asserting the claim to be anticipated by U.S. Patent No. 4,313,174 to White.

White, however, fails to disclose each of the features of Applicant's invention. For example, White neither explicitly nor inherently teaches a folding multiplier that effects the folding process as taught by Applicant's invention. White is explicitly directed to obtaining the square, C^2, of a value, C, and to performing digital multiplication by means of the quarter-square method. (Col. 3, Lines 20-24; Col. 5, lines 15-23.) The arithmetic device for squaring values is described as a square function ROM and comprises separate, parallel ROMs **11**, **12**, **13** along with "gain-scaling means" **17** and **18** connected with the ROMs. (Col. 3, line 57 – Col. 4, line 51; Col. 5, Lines 15-48; FIG. 1-FIG. 3.)

Operationally, the value C is applied to a 16-bit parallel digital input in such a manner that the digital input's most significant bits (MSB) are directed to one of the ROMs and its least significant bits (LMB) are directed to another. (Col. 4, Lines 6-13.) The two inputs are designated C_m and C_l, respectively. The two inputs, along with a

sum of the two inputs, are subsequently supplied to and squared by the ROMs. The outputs of the ROMs, specifically, are C_m^2, C_l^2, and $(C_m^2 + C_l^2)$. (Col. 4, Line 13.) The outputs are then scaled by the gain-scaling means and supplied to a digital summer to yield ultimately the following result for the desired squared value: $C^2 = \left[2^{N/2} C_m + C_l\right]^2 = 2^N C_m^2 + 2^{N/2+1} C_m C_l + C_l^2$.

The differences in the algebraic steps effected by White and with Applicant's invention underscore fundamental differences in the structure and operation of White's device and Applicant's invention. As noted, White relies on a plurality of ROMs in conjunction with scaling means and a summer for effecting the desired arithmetic operations. By contrast, Applicant's invention provides a high-speed scalable multiplier using a folding multiplier. Accordingly, there are significant structural differences between White's ROM-based device and Applicant's high-speed scalable multiplier with folding multiplier. Among the advantages that follow from Applicant's invention is that larger sized multipliers (i.e., ones handling larger bit-sized data) can be obtained using smaller sized ones. (See, e.g., Specification, pp. 8-9.)

Moreover, Applicant's invention further provides a folding process using a multiplier-implemented algorithm. It is not apparent from White how the algorithm implemented using multiple ROMs can be adapted to perform Applicant's folding process, which can implemented in the folding multiplier of Applicant's invention.

Another aspect of Applicant's invention that is not taught or suggested by White is a high-speed scalable multiplier having at least one multiplier and at least one folding multiplier along with at least one decoder for dynamically selecting a multiplier and folding multiplier. The dynamic selection afforded by Applicant's invention can be in response to changing conditions related to factors such as an increased need for power

efficiency. (See, e.g., Specification, p. 12.) A comparable capability is not taught or suggested by White.

Applicant respectfully asserts, therefore, that the prior art fails to teach or suggest each feature recited in independent Claims 7, 9, and 11. Moreover, Applicant further respectfully maintains that the prior art likewise fails to teach or suggest each feature recited in dependent Claims 8, 10, and 12.

III. Amended FIG. 9

As noted above, FIG. 9 has been amended. The amendment removes decision blocks 110 and 116 the designation "*F" in each of the blocks. The designation was intended to connote that the scaling factor, in terms of a digital representation, is a concatenation, hence the use of "*" in the designation. The dropping of the designation is more consistent with decision blocks 112 and 114, and is likewise more consistent with the description of each scaling factor being either zero or one depending on whether the multiplicand or multiplier, respectively, or both, is to be reduced in size by the folding process.

CONCLUSION

Applicant believes that this application is now in full condition for allowance, which action is respectfully requested. Applicant requests that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the

Examiner believes a telephone interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

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[MARKED-UP SHEET]

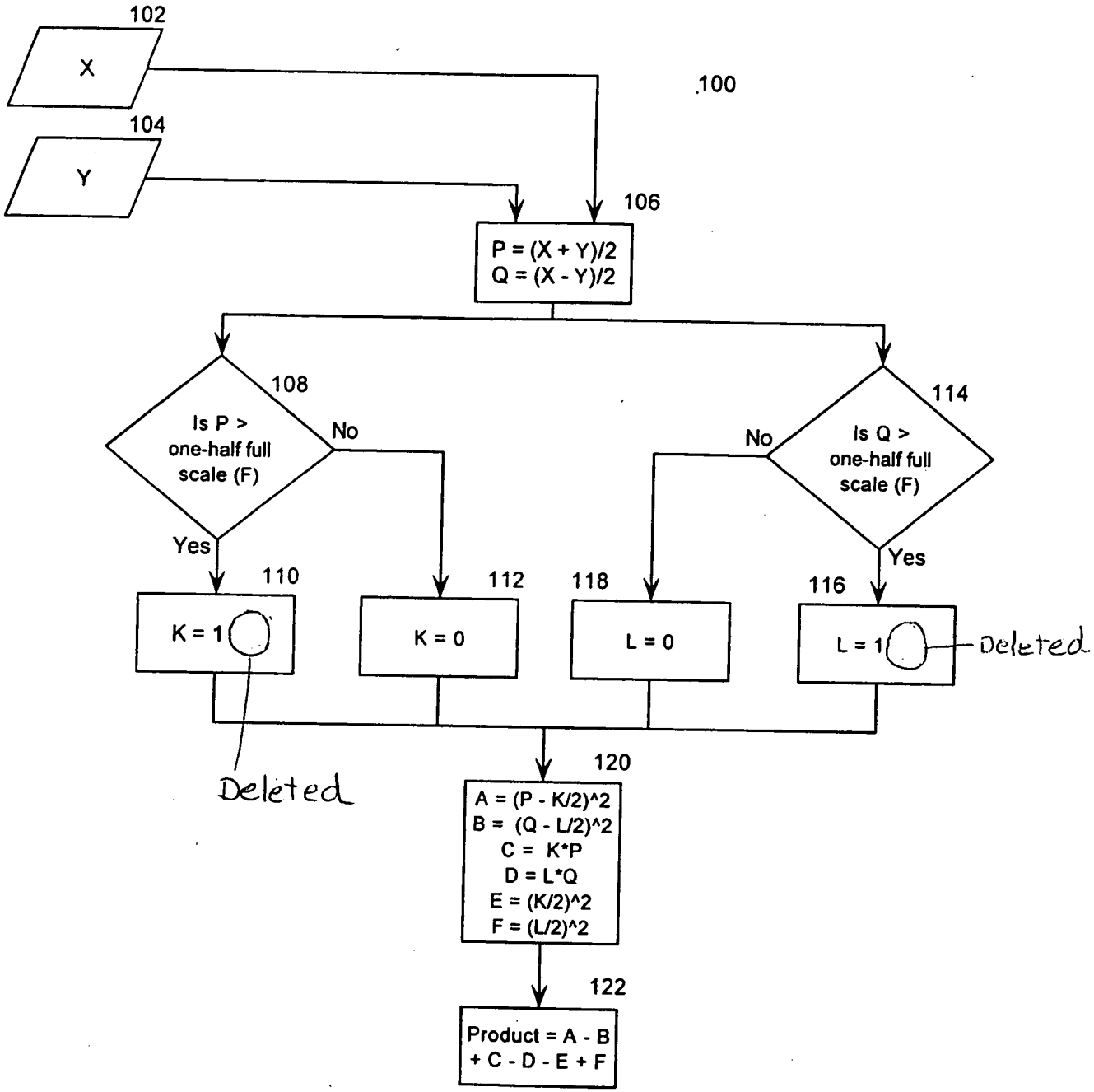

Fig. 1